OTFL101-EVAL Datasheet

Features

- Evaluation board for the OTFL101 Ultra Linear 2.5 – 7.5 GHz Tunable Filter Evaluation Board
- Embedded microcontroller with Otava software GUI
- Header provided for external control
- TRL calibration structures included

Description

The OTFL101-EVAL is designed for the user to evaluate the performance of the OTFL101 2.5 – 7.5 GHz Tunable Filter. Please refer to the OTFL101 datasheet for full details on the filter.

Required External Equipment

- Network Analyzer
- USB-C Cable
- Windows PC
- Otava Software GUI (supplied)

Applications

- Aerospace & Defense
- Wireless Infrastructure
- Satellite Communication
- Instrumentation
- Automotive

OTFL101 Evaluation Board

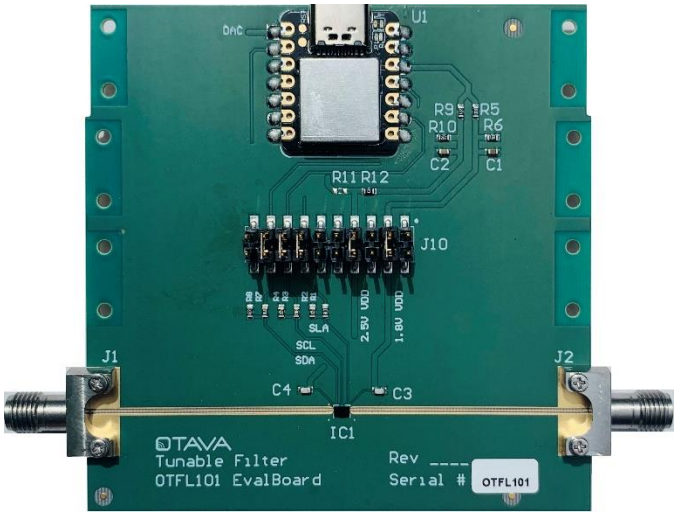

Figure 1 – OTFL101-EVAL Evaluation Board

OTFL101 Block Diagram

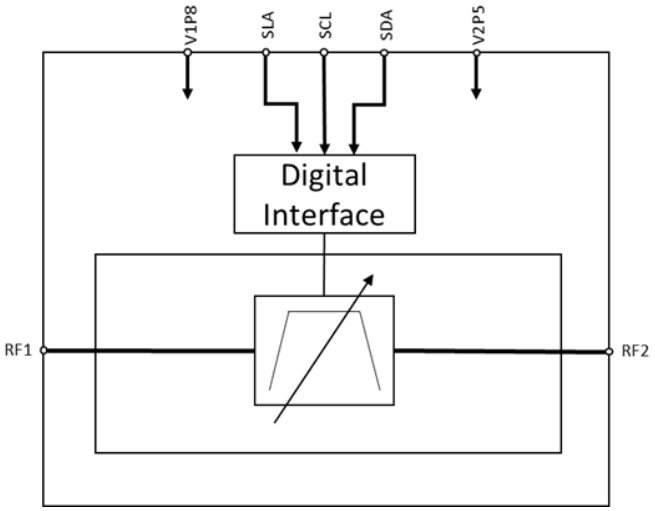

Figure 2 – OTFL101 IC Block Diagram

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Revision History

August 2021, RevA (Initial Release)

Evaluation Board Overview

The evaluation board is shown above in Figure 1 – OTFL101-EVAL Evaluation Board. Compression mounted SMA connectors are utilized on the board for the two filter ports. The board includes a Seeeduino microcontroller to control the filter's bits. A header is provided in case the user wants to connect their own test equipment to control the filter, bypassing the Seeeduino. TRL calibration structures are provided on the bottom of the board (Thru, Line, and Short); connectors for these paths are not provided and must be purchased separately.

The board consists of 4 layers and is detailed below:

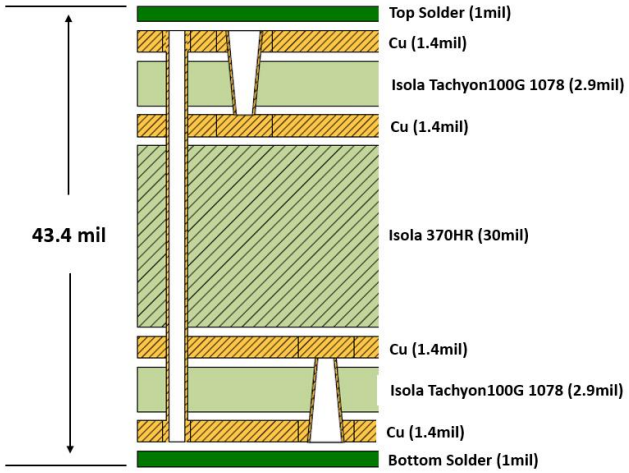

Figure 3 – OTFL101-EVAL PCB Stackup

The gerber files of the evaluation board are provided to assist the user in the implementation of the filter IC.

RF I/O Signals

The filter RF paths are routed on the top layer of the board. The TRL calibration paths are routed on the bottom layer. All RF lines are designed using a CPWG (coplanar waveguide) structure, with a trace width of 7 mil (tapered to 5mils going into the filter I/O pads) and ground spacing of 9.5 mil. All RF I/Os are 50Ω nominal.

Table 1 – RF Connector I/O

Connector	I/O	Description
J1	RF1	Filter RF Port 1
J2	RF2	Filter RF Port 2
J3	Short P1	Short Calibration Port1
J4	Short P2	Short Calibration Port2
J5	Line P1	Transmission Line Port1
J6	Line P2	Transmission Line Port2
J7	Thru P1	Thru Line Port1
J8	Thru P2	Thru Line Port2

Testing the Filter

Below is a typical setup to measure the s-parameters of the filter:

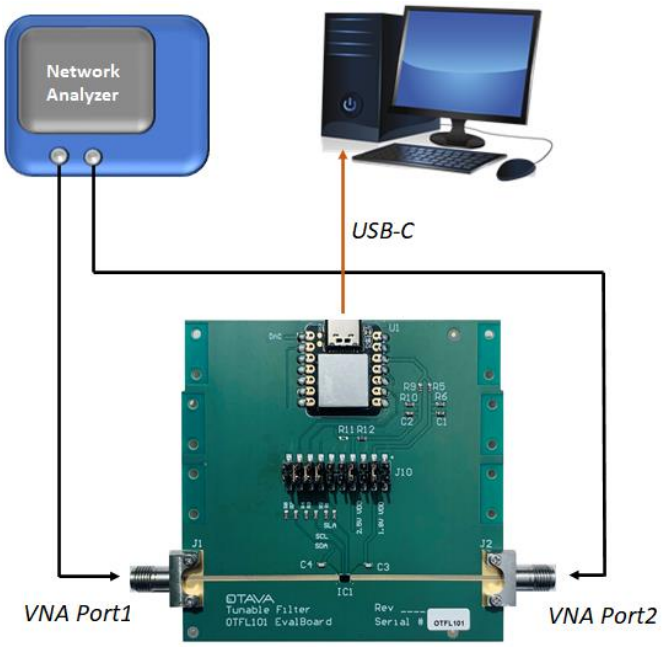

Figure 4 – OTFL101-EVAL Filter Test Setup

Two ports of a network analyzer are used to measure the small signal response when connecting the VNA port 1 to the J1 connector, and VNA port 2 to the J2 connector of the evaluation board.

A USB-C cable is used to connect the Seeeduino (U1) to the test PC. The Seeeduino is then powered up from this connection. +3.3V is passed to the PCB from the Seeeduino (Pin12) and that is used to generate the required +1.8V (resistor divider formed from R5 and R6) and +2.5V (resistor divider formed from R9 and R10) power supplies for the filter.

The Seeeduino also generates the required digital signals to control the filter. The clock (pin 15), data (pin 17), and latch (pin 13) signals are routed to the control header, J10. Each of these signals go through a resistor divider on the board which lowers the +3.3V logic level coming out of the Seeeduino to +1.8V for the tunable filter interface.

Five jumpers are utilized to short the pins of the Seeeduino control signals and PCB created voltages to the filter I/O. The board is provided with the jumpers in place. Refer to the table below for the jumper setup.

Table 2 – J10 Control Header (Using Seeeduino)

Pin	I/O	Description	Jumper
1	GND	Ground	
2	GND	Ground	
3	VDD_1	1.8V	x
4	VDD_1		
5	GND	Ground	
6	GND	Ground	
7	VDD_2	2.5V	x
8	VDD_2		
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	A1	SLA	x
14	A1_VD		
15	A8	SCL	x
16	A8_VD		
17	A10	SDA	x
18	A10_VD		
19	GND	Ground	
20	GND	Ground	

An Otava designed software GUI is provided to control the filter through the Seeeduino, which is pre-programmed. Once the connection is made between the Seeeduino and PC via the USB-C cable, launch the GUI (filter_control_gui_v0p1.exe).

The opening screen is shown below. Select the appropriate COM port from your PC to establish initial communication to the Seeeduino device:

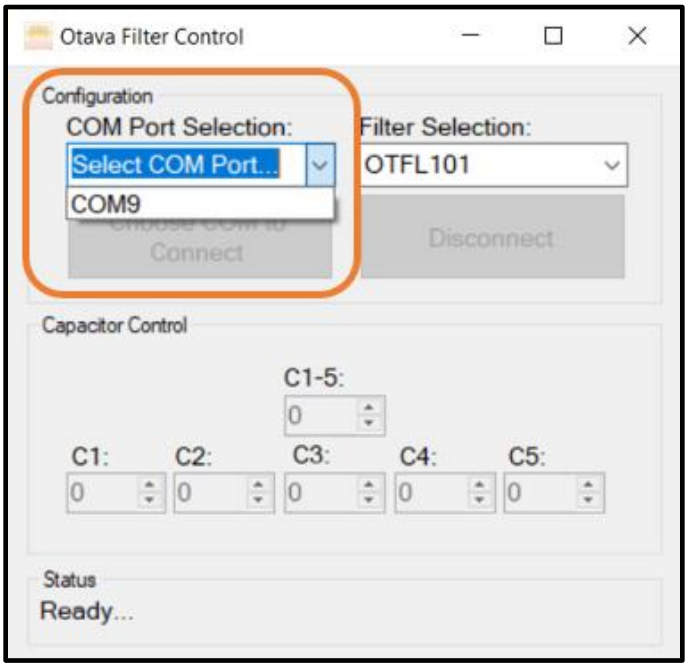

Figure 5 – GUI Opening Screen

Once the COM port is selected and the 'Connect' button is pressed, the 'Status' message on the bottom of the window will display the following message that the port is opened:

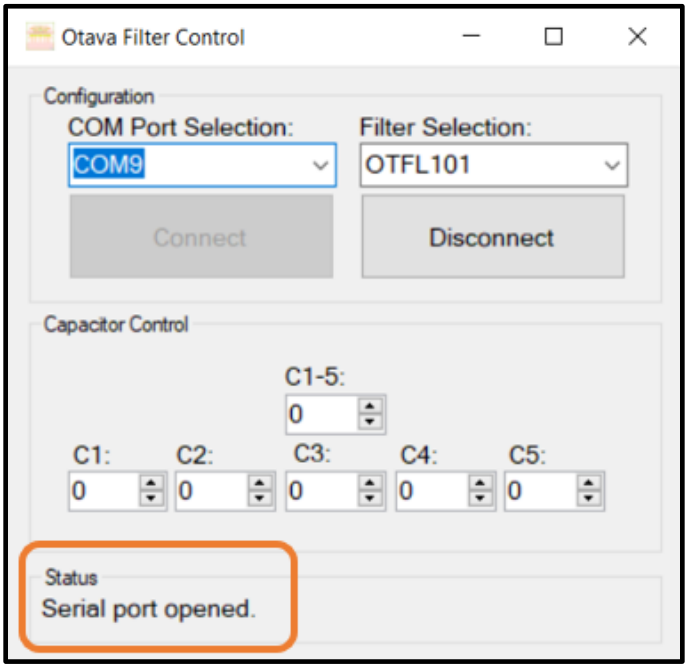

Figure 6 – GUI Establishing Communications

This software is utilized for the family of tunable filters that Otava currently has available (OTFL101, OTFL201, OTFL301). For this evaluation board design, the OTFL101 will be used under the Filter Selection drop down menu:

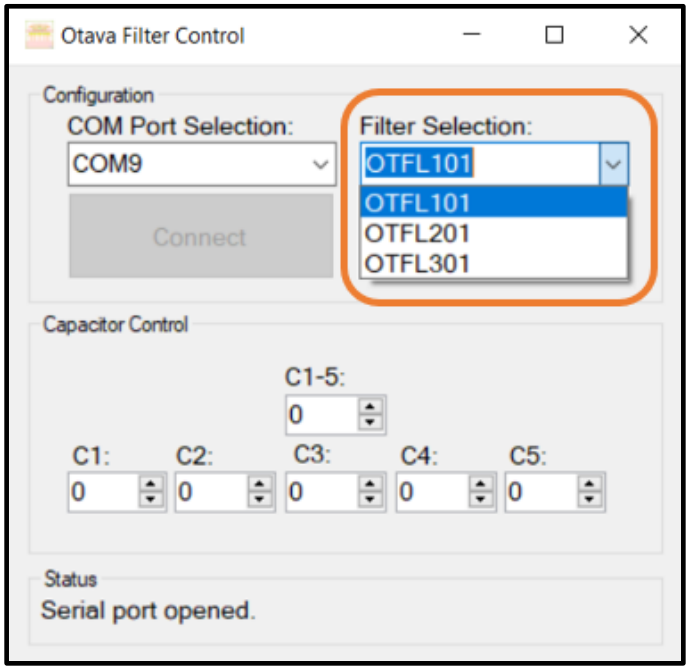

Figure 7 – GUI Filter Selection

To control the capacitor banks of the filter, each of the five stages are broken out from C1 to C5. The C1-5 control will toggle all filter stages at the same time. The changes are automatically applied each time the values are updated. A status message will be displayed on the bottom of the window each time the values are changed:

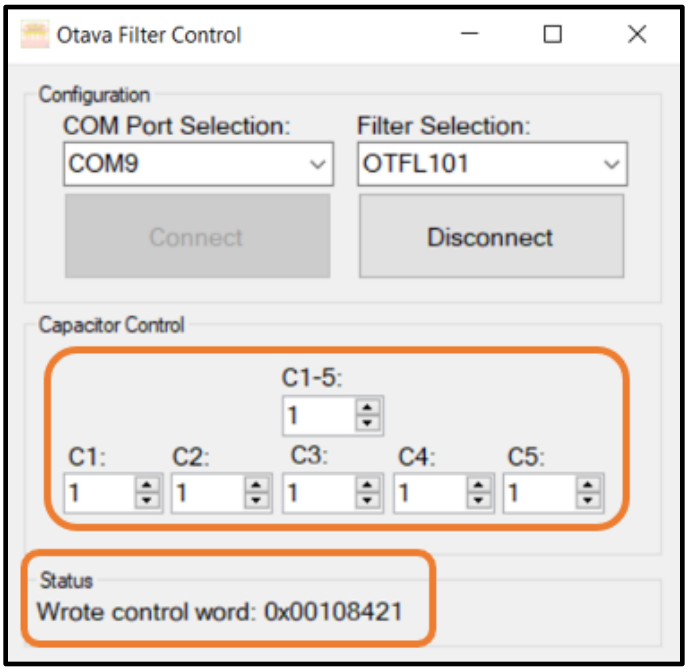

Figure 8 – GUI Control Applied

If the user would want to utilize their own test control equipment, the jumpers can be removed, and the five required connections will become available to hook in external connections, as detailed in the below table (pins 4,8,14,16, and 18):

Table 3 – J10 Control Header (Bypassing Seeeduino)

Pin	I/O	Description
1	GND	Ground
2	GND	Ground
3	VDD_1	not used
4	VDD_1	Connect external 1.8V
5	GND	Ground
6	GND	Ground
7	VDD_2	not used
8	VDD_2	Connect external 2.5V
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	A1	Ground
14	A1_VD	Connect external SLA
15	A8	not used
16	A8_VD	Connect external SCL
17	A10	Ground
18	A10_VD	Connect external SDA
19	GND	Ground
20	GND	Ground

Additional Information

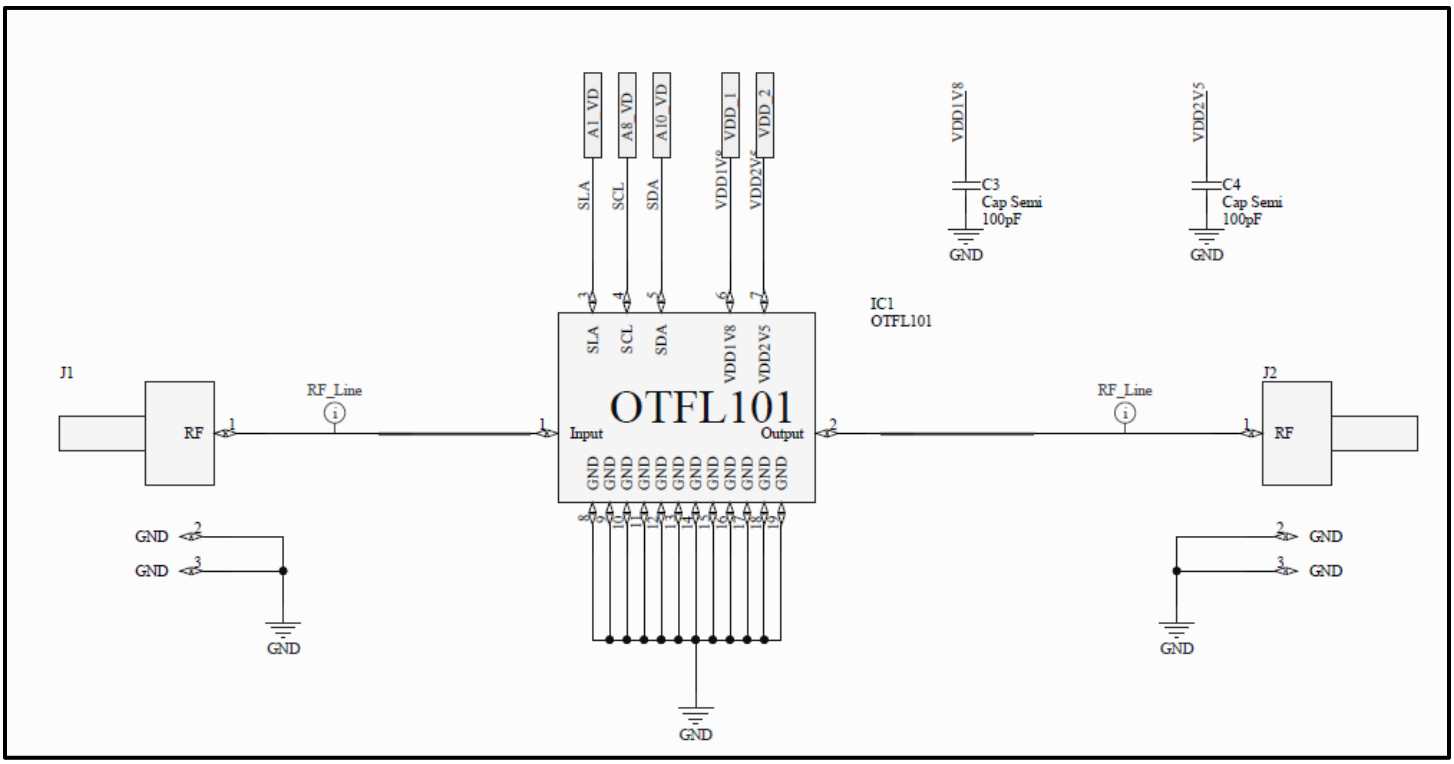

Figure 9 – OTFL101-EVAL Schematic (Filter – 1 of 2)

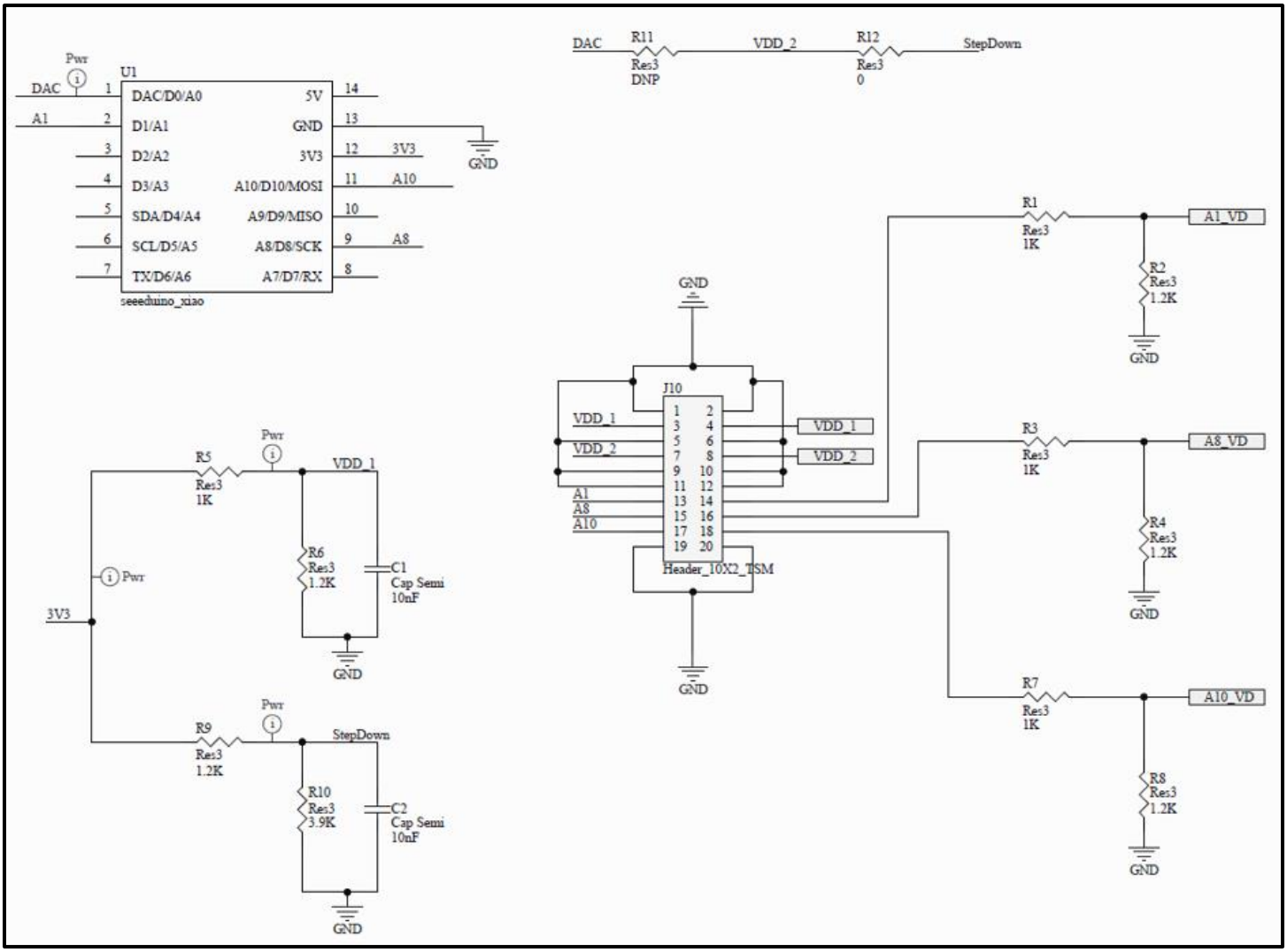

Figure 10 – OTFL101-EVAL Schematic (Control – 2 of 2)

Table 4 – Bill of Materials, OTFL101-EVAL

Reference Designator	Qty	Description	Part Number	Vendor
--	1	Evaluation PCB	OTFL101-PCB	Otava
IC1	1	Tunable Filter, 2.5 - 7.5 GHz	OTFL101	Otava
U1	1	Microcontroller	Seeeduino Xiao	Seeed
J1, J2, (J3-J8 not supplied)	2	Compression edgemount SMA RF Connector	TMB-E5F2-1L1	CarlisleIT
J10	1	Header SMD 20 Pos 2.54mm	TSM-110-01-F-DV	Samtec
R1, R3, R5, R7	4	Resistor SMD 1K OHM 1% 1/10W 0603	RC0603FR-071KL	Yageo
R2, R4, R6, R8, R9	5	Resistor SMD 1.2K OHM 1% 1/10W 0603	RC0603FR-071K2L	Yageo
R10	1	Resistor SMD 3.9K OHM 1% 1/10W 0603	RC0603FR-073K9	Yageo
R12	1	Resistor SMD 0 OHM JUMPER 1/10W 0603	RC0603JR-070RL	Yageo
C1, C2	2	Capacitor CER 0.1UF 100V X7R 0603	CC0603KRX7R0BB104	Yageo
C3, C4	2	Capacitor CER 100PF 25V NPO 0603	CC0603JRNPO8BN101	Yageo
J10-x	5	Shorting Jumpers for J10	SPC02SXCN-RC	Sullins

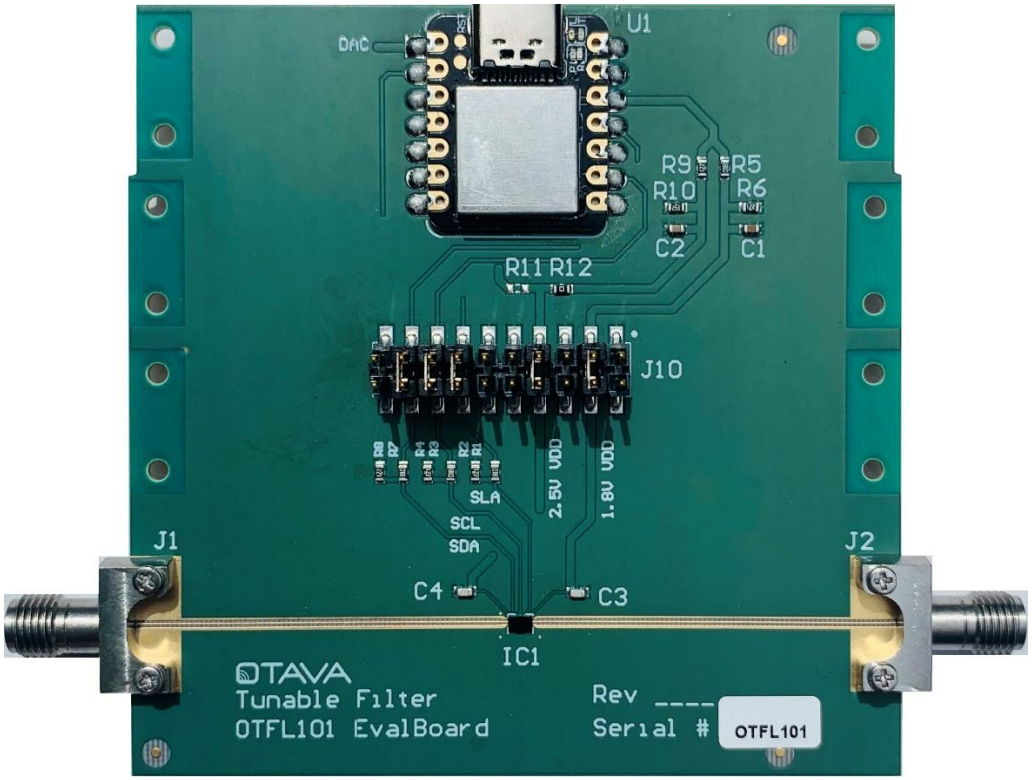

Figure 11 – OTFL101-EVAL PCB (Top)

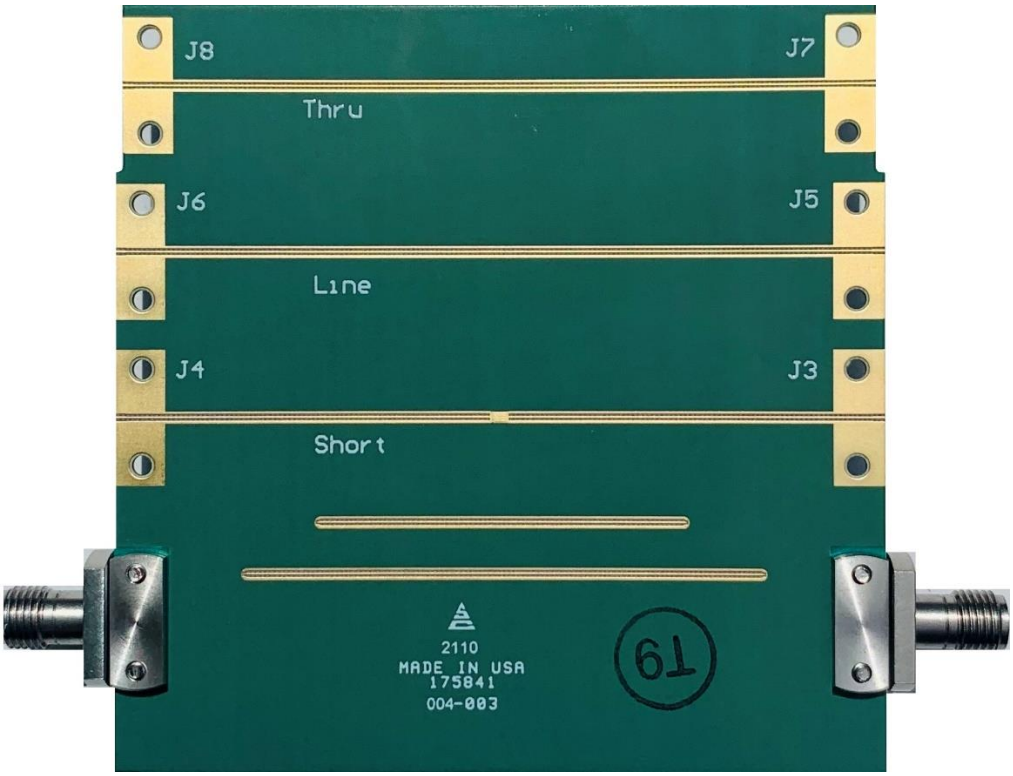

Figure 12 – OTFL101-EVAL PCB (Bottom)

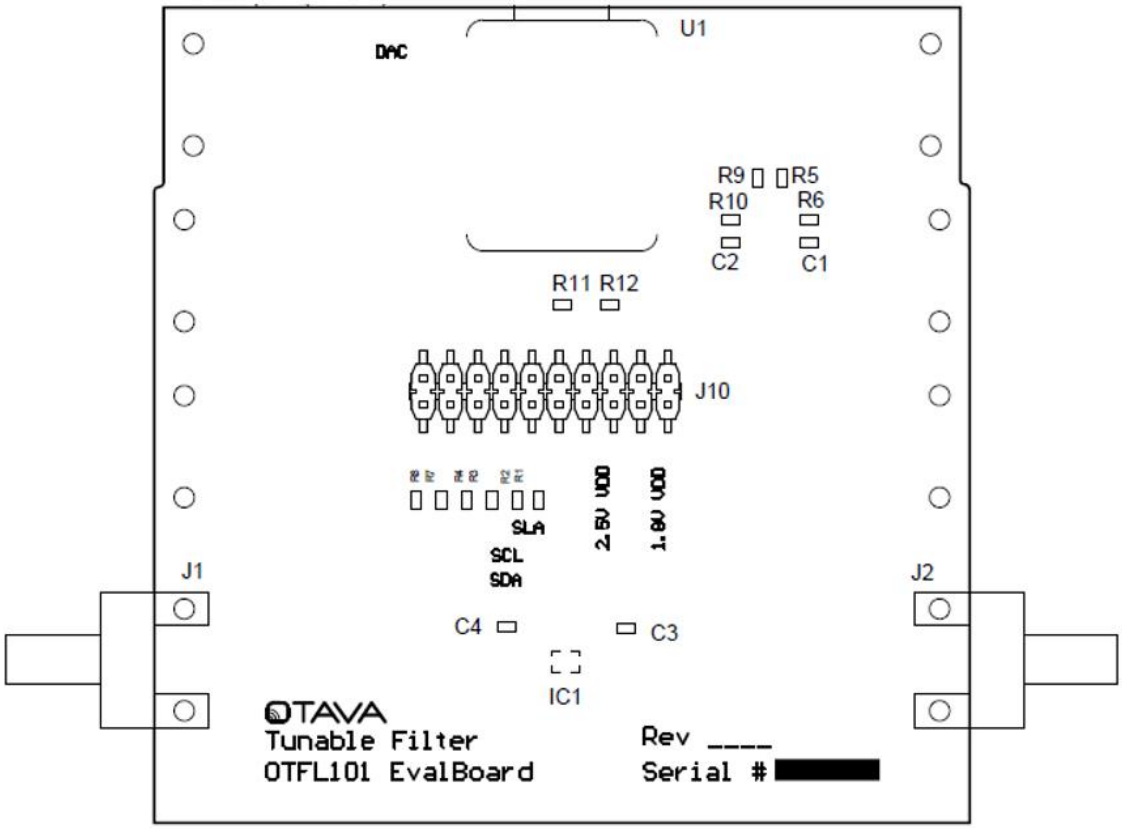

Figure 13 – OTFL101-EVAL Assembly Drawing (Top)

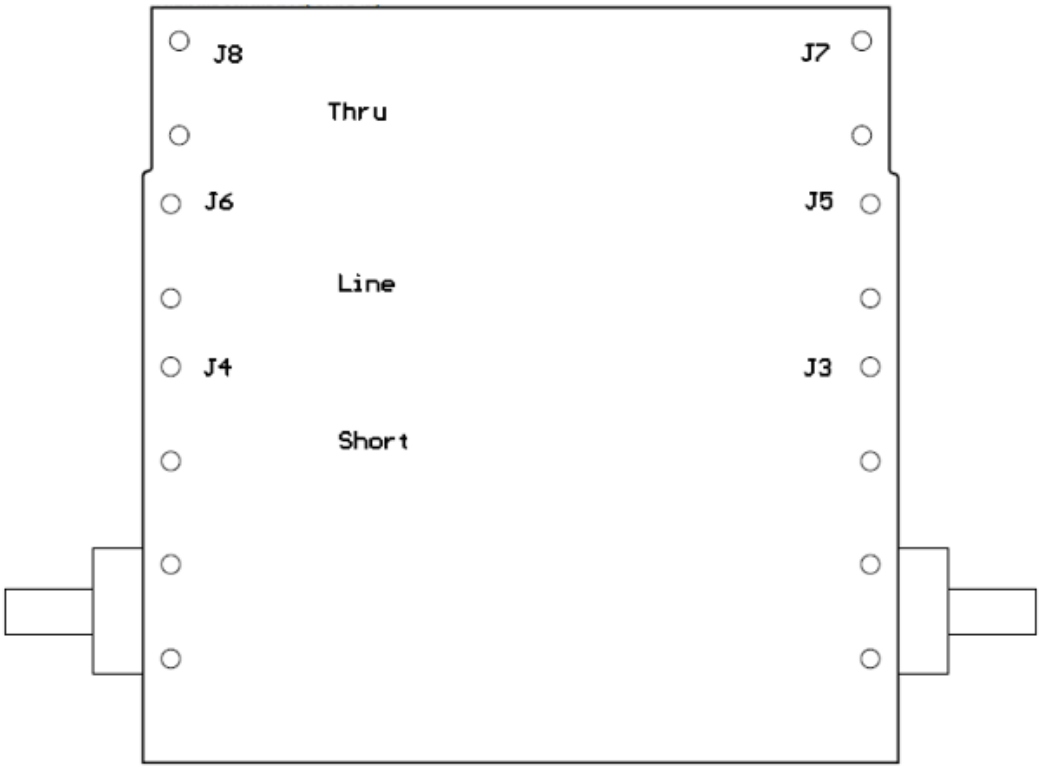

Figure 14 – OTFL101-EVAL Assembly Drawing (Bottom)