OTSW100 Datasheet

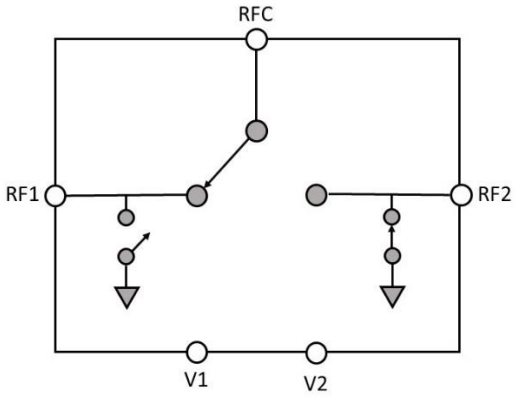
Features

- DC to 40 GHz Frequency Range
- Insertion Loss: < 1.5 dB
- Isolation: > 35 dB
- IIP3: > 40 dBm
- Switching Time: 175 ns typical
- Control Voltage: +/- 2.5 V
- SOI Technology
- Flip Chip C4 Bump
- Die Dimension: 2.546 mm x 2.161 mm

Description

The OTSW100 is a wideband SPDT RF switch that operates from DC to 40 GHz. This switch features low insertion loss, high isolation, fast switching time and high linearity up to 40 GHz, making the switches ideal to be utilized in application platforms such as wireless infrastructure, aerospace & defense, satellite communication, instrumentation and automotive.

Block Diagram



Applications

- Aerospace & Defense
- Wireless Infrastructure
- Satellite Communication
- Instrumentation
- Automotive

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Revision History

August 2021, RevA (Initial Release)

November 2021, RevB (Timing Performance Update)

Specifications

For all supplied data in the table below, the nominal conditions are defined as the following:

- Ambient Temperature: 25°C
- V1 = 2.5V, V2=-2.5V or V1 = -2.5V, V2 = 2.5V
- Measured on the OTSW100-EVAL evaluation board and de-embedded using Automatic Fixture Removal (AFR)

Table 1 – Specifications

Parameter	Test Configuration	Units	Min.	Typ.	Max.
Operating Temperature		°C	-40	25	105
Operating RF Frequency		GHz	DC		40
Insertion Loss					
100MHz	RFC to RF1/RF2	dB		0.33	
100 MHz - 26.5 GHz		dB		1.15	
26.5 GHz - 40GHz		dB		1.5	
Return Loss (RFC Port)					
100MHz	RFC to RF1/RF2	dB		30	
100 MHz - 26.5 GHz		dB		12	
26.5 GHz - 40GHz		dB		12.5	
Return Loss (RF1/RF2 Port)					
100MHz	RFC to RF1/RF2	dB		30	
100 MHz - 26.5 GHz		dB		11	
26.5 GHz - 40GHz		dB		7.5	
Isolation					
100MHz	All Port to Port	dB		90	
100 MHz - 26.5 GHz		dB		44	
26.5 GHz - 40GHz		dB		35	
IP1dB	> 100 MHz	dBm	30		
IIP3	>100MHz	dBm	40		
RF Trise/Tfall	10%/90% RF	ns		50	
Settling Time	50% CTRL to within 0.05dB final value	ns		200	
Switching Time	50% CTRL to 10% or 90% RF	ns		175	

Absolute Maximum Ratings

Table 2 – Absolute Maximum Ratings

Parameter	Rating
V1, V2 Maximum Positive Voltage	+3V
V1,V2 Maximum Negative Voltage	-3V
Maximum RF Input Power	TBD
Junction Temperature	+125C
Storage Temperature Range	-65C to +150C
c4 Reflow	260C
Electrostatic Discharge	
Digital Pins (HBM)	2000 V
RF Pins (HBM)	1000 V

Switch Control Logic

Table 3 – Switch Control Logic Truth Table

V1	V2	RF1	RF2	State
-2.5V	-2.5V	OFF	OFF	1
-2.5V	+2.5V	OFF	ON	2
+2.5V	-2.5V	ON	OFF	3
+2.5V	+2.5V	ON	ON	4

Typical Performance Plots

For all supplied data in the table below, the nominal conditions are defined as the following:

- Ambient Temperature: 25°C
- V1 = 2.5V, V2=-2.5V or V1 = -2.5V, V2 = 2.5V
- Measured on the OTSW100-EVAL evaluation board and de-embedded using Automatic Fixture Removal (AFR)

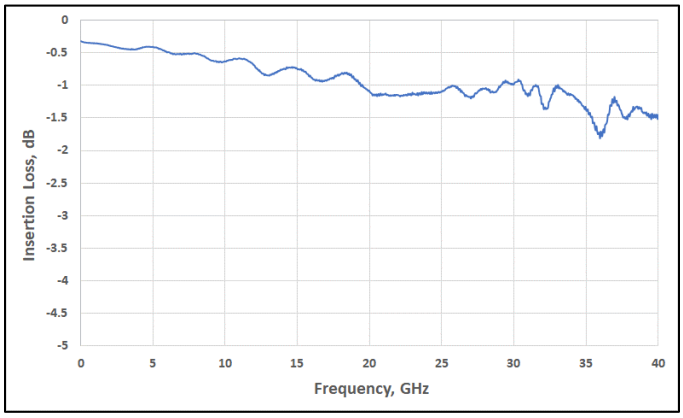

Figure 1 – Insertion Loss for RF1/RF2 Paths

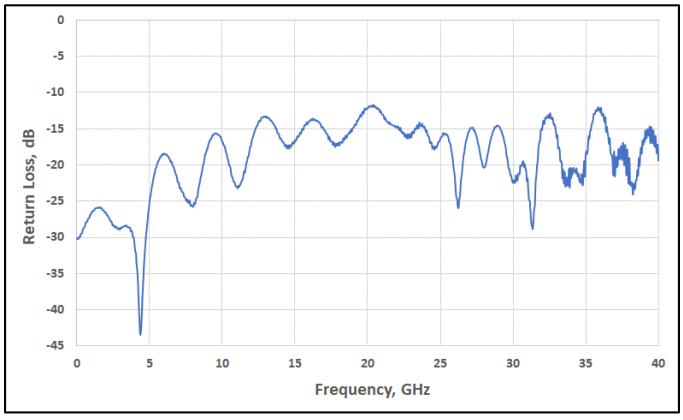

Figure 2 – RFC Port Return Loss

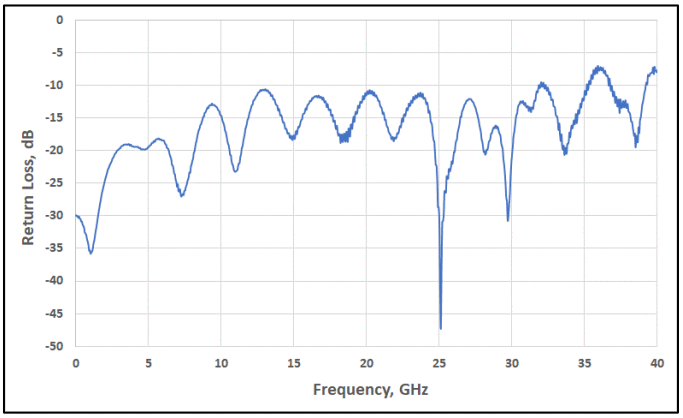

Figure 3 – RF1/RF2 Port Return Loss

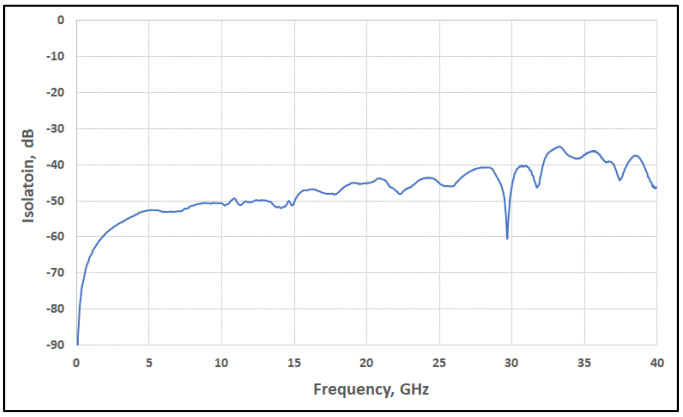

Figure 4 – Isolation RF1-RF2

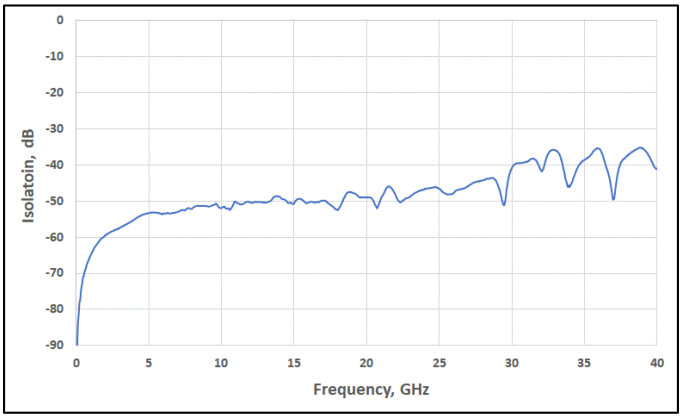

Figure 5 – Isolation RFC to RF1/RF2

I/O Functional Description

Table 4 – Switch Pin Description

Pin	Name	Description
1	RF2	RF Port 2 (50Ω)
2	RF1	RF Port 1 (50Ω)
3	RFC	Common RF Port (50Ω)
4	V1	Control Input 1
5	V2	Control Input 2
6-19	GND	Ground

Pin Configuration

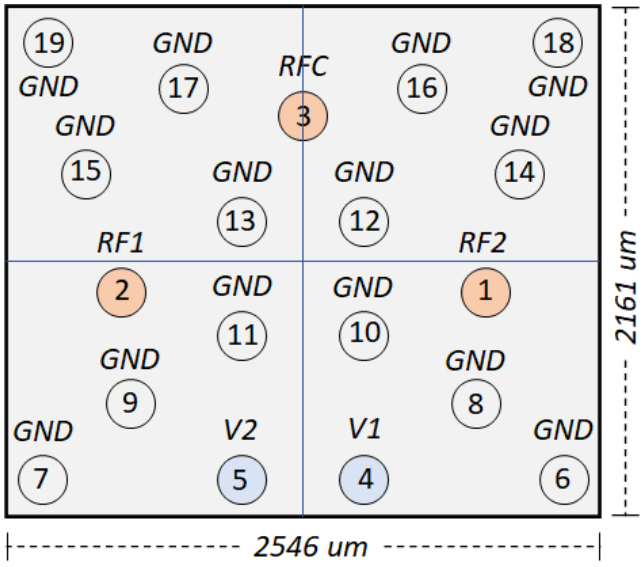

Figure 6 – Pin Configuration (Bumps Up)

Note: Drawing not drawn to scale.

Table 5 – Pin Coordinates

Pin	Name	Pin Center (um)	
		X	Y
1	RF2	785.5	-121.5
2	RF1	-785.5	-121.5
3	RFC	0	629
4	V1	253.5	-958.5
5	V2	-253.5	-958.5
6	GND	1128.5	-958.5
7	GND	-1128.5	-958.5
8	GND	731.5	-646.5
9	GND	-731.5	-646.5
10	GND	253.5	-326.5
11	GND	-253.5	-326.5
12	GND	253.5	183.5
13	GND	-253.5	183.5
14	GND	931.5	363.5
15	GND	-931.5	363.5
16	GND	503.5	753.5
17	GND	-503.5	753.5
18	GND	1091.5	913.5
19	GND	-1091.5	913.5

Note: All coordinates are referenced to the die center and refer to the center of the pin.

Die Mechanical Specifications

Table 6 - Die Mechanical Specifications

Parameter	Unit	Min	Typ	Max	Notes
Die size (x,y)	um		2546x2161		+/- 10um
Die thickness	um		300		
Bump Material	-		SnAg		
Bump Pitch	um	500			
Bump Height	um		75		
Bump Diameter	um		90		

The die minimum pitch of 500um allows for integration onto standard RF PCB materials. Soldermask defined pads are utilized for the bump landing areas. Please refer to the supplied Altium footprint file and the OTSW100-EVAL evaluation board artwork files for the exact landing pattern dimensions and implementation.