

Introduction

This assembly guide describes the recommended footprint and assembly process for implementing the OTFL101, OTLF201, and OTFL301 tunable filters onto a printed circuit board (PCB).

Description

The OTFL101, OTFL201, and OTFL301 are digitally tunable bandpass filters that operate between the frequencies of 2.5 to 40 GHz. They offer high IIP3 performance in a miniaturized footprint. The filter I/Os are connected to standard PCB materials using lead-free solderballs.

These devices provide solutions for systems that need to remove spurs or unwanted signals/interferences and replace switched filter banks. Application areas include but not limited, radio, communication, military radar, automotive, and instrumentation.



Figure 1 – OTFL101 Eval Board PCB Footprint

Overview

The OTFL101 has a minimum pitch of 280 um between all RF, control, and ground pins. The signal I/Os are placed around the perimeter of the die to facilitate integration onto standard PCB materials. The size of the die is 2.340 mm x 1.634 mm.

The OTFL201 and OTFL301 share the same footprint and have a minimum pitch of 280 um between all RF, control, and ground pins. The signal I/Os are placed around the perimeter of the die to facilitate integration onto standard PCB materials. The size of the die is 1.634 mm x 1.637 mm.



Figure 2 – OTFL201/301 Eval Board PCB Footprint

Evaluation Board Footprint



Figure 3 – OTFL101 Eval Board PCB Footprint (Altium)



Figure 4 – OTFL201/301 Eval Board PCB Footprint (Altium)

The evaluation board is constructed with standard PCB materials. Please refer to the evaluation board datasheets for more details.

In Figures 3 and 4, the top layer artwork is displayed in the Altium Designer CAD tool. The red is the top layer metal, the purple circles are the top layer soldermask openings, and the yellow is the top silkscreen layer. Please refer to the supplied footprint files for exact dimensions of the feature sizes. Figures 1 and 2 show the fabricated PCB top layer for the filters.

PCB Soldermask Rules

It is important that the top layer soldermask placement is well controlled on the PCB. This is accomplished by ensuring that on the PCB fabrication drawing, the soldermask defined pad opening areas are called out within an allowable tolerance of +/-1 mil or better. The registration to the top layer is also key, +/-1 mil or better, so that the soldermask is accurately placed in the footprint area of the device. Laser Direct Image (LDI) soldermask accomplishes this, and there are Liquid Photo Imageable (LPI) processes that can achieve this as well. Consult with your PCB fabrication vendor for the best selection for your design and to verify the tolerances they can hold to.

Finally, the maximum thickness of the soldermask must be defined as < 1.2 mils to ensure that it is not touching the face of the chip and propping it up, inhibiting the reflow of the solderballs to the PCB.

Reflow to the PCB

The SnAg solderballs of the IC are to be dipped into flux before the component is reflowed onto the PCB. Solder paste is not applied to the board I/O pads of the device due to the bump pitch and size of the bumps. The reflow profile for the IC to the PCB follows published JEDEC standard, J-STD-020D.1 (lead free reflow Table 4-2).

The maximum reflow temperature shall not exceed +260°C. See Figure 5 below as a guide for the reflow profile. Consult with your surface mount assembly vendor to refine the reflow profile, which considers the other component requirements on the board and PCB substrate material properties.

Underfill is not required to be used between the attached filter and PCB. However, if the application requires it, be sure to use a low loss, low dielectric constant material to not impact the performance of the device.

Conclusion

This document is provided to aide in ensuring a successful attachment of the filter IC to a PCB. The rules and requirements are made available from the evaluation board product designs, which are constructed with standard PCB materials.



Figure 5 – Reflow Profile for Tunable Filter IC Attachment