OTSW100/101 Attachment Guide

Introduction

This assembly guide describes the recommended footprint and assembly process for implementing the OTSW100 and OTSW101 switches onto a printed circuit board (PCB).

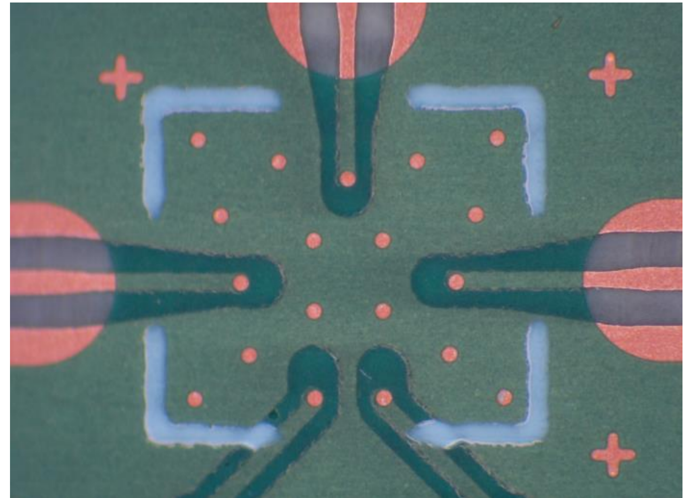

Figure 1 – OTSW100 Eval Board PCB Footprint

Description

The OTSW100 and OTSW101 are wideband SPDT RF switches that operate from DC to 40 GHz. These devices feature low insertion loss, high isolation, fast switching time and high linearity up to 40 GHz, making the switches ideal to be utilized in application platforms such as wireless infrastructure, aerospace & defense, satellite communication, instrumentation and automotive. The switch I/Os are connected to standard PCB materials using lead-free solderballs.

Overview

The OTSW100 features a minimum pitch of 500um between all RF, control, and ground pins to facilitate an easy integration onto standard PCB materials. The size of the die is 2.546 mm x 2.161 mm.

The OTSW101 is a reduced footprint version of the OTSW100, offering comparative performance in a smaller footprint. The size of the die is 1.634 mm x 1.637 mm.

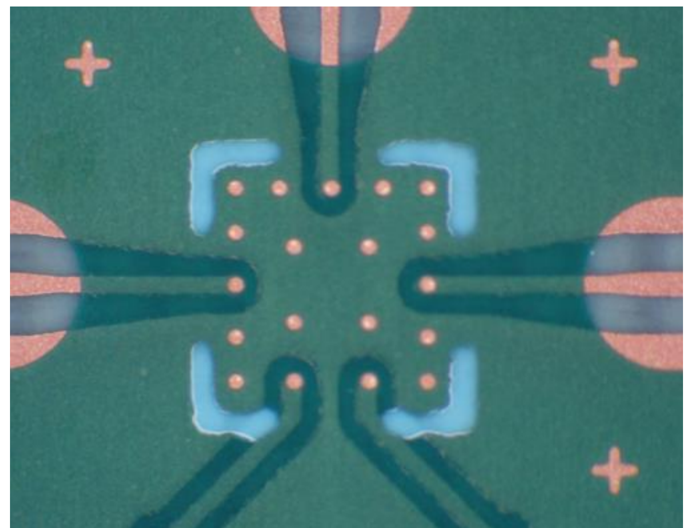

Figure 2 – OTSW101 Eval Board PCB Footprint

Evaluation Board Footprint

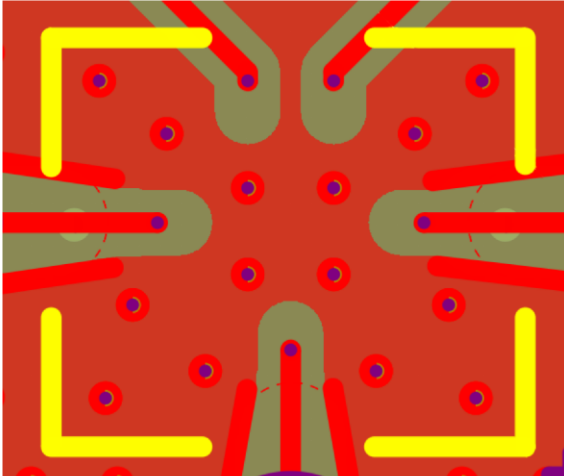

Figure 3 – OTSW100 Eval Board PCB Footprint (Altium)

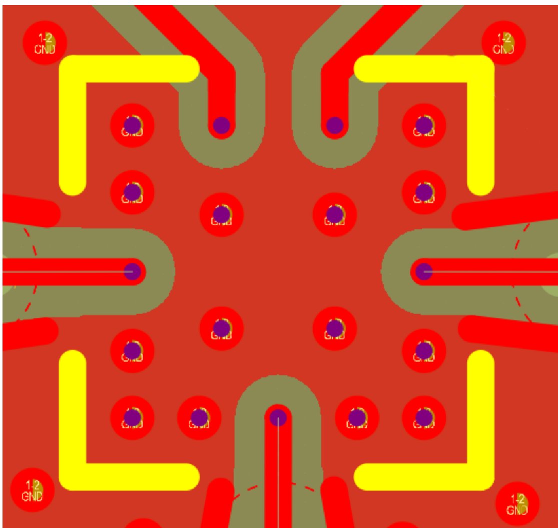

Figure 4 – OTSW100 Eval Board PCB Footprint (Altium)

The evaluation board is constructed with standard PCB materials. Please refer to the evaluation board datasheet for more details.

In Figured 3 and 4, the top layer artwork is displayed in the Altium Designer CAD tool. The red is the top layer metal, the purple circles are the top layer soldermask openings, and the yellow is the top silkscreen layer. Please refer to the supplied footprint files for exact dimensions of the feature sizes. Figures 1 and 2 show the fabricated PCB top layer for the switches.

PCB Soldermask Rules

It is important that the top layer soldermask placement is well controlled on the PCB. This is accomplished by ensuring that on the PCB fabrication drawing, the soldermask defined pad opening areas are called out within an allowable tolerance of +/-1 mil or better. The registration to the top layer is also key, +/-1 mil or better, so that the soldermask is accurately placed in the footprint area of the device. Laser Direct Image (LDI) soldermask accomplishes this, and there are Liquid Photo Imageable (LPI) processes that can achieve this as well. Consult with your PCB fabrication vendor for the best selection for your design and to verify the tolerances they can hold to.

Finally, the maximum thickness of the soldermask must be defined as < 1.2 mils to ensure that it is not touching the face of the chip and propping it up, inhibiting the reflow of the solderballs to the PCB.

Reflow to the PCB

The SnAg solderballs of the IC are to be dipped into flux before the component is reflowed onto the PCB. Solder paste is not applied to the board I/O pads of the device due to the bump pitch and size of the bumps. The reflow profile for the IC to the PCB follows published JEDEC standard, J-STD-020D.1 (lead free reflow Table 4-2).

The maximum reflow temperature shall not exceed +260°C. See Figure 5 below as a guide for the reflow profile. Consult with your surface mount assembly vendor to refine the reflow profile, which considers the other component requirements on the board and PCB substrate material properties.

Underfill is not required to be used between the attached switch and PCB. However, if the application requires it, be sure to use a low loss, low dielectric constant material to not impact the performance of the device.

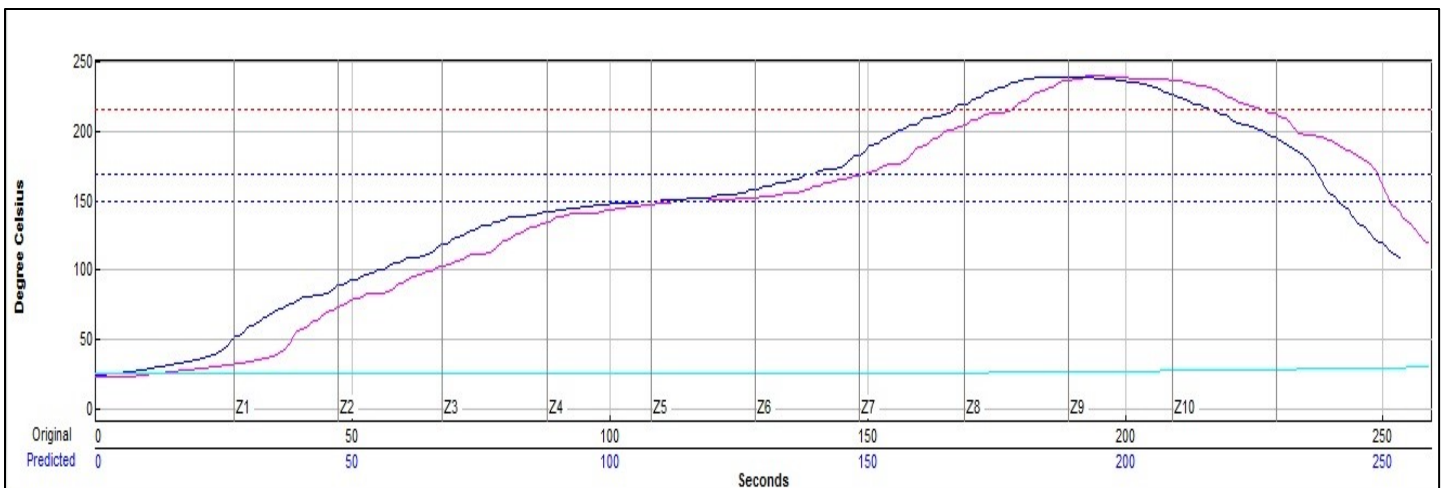

Figure 5 – Reflow Profile for Switch IC Attachment

Conclusion

This document is provided to aide in ensuring a successful attachment of the switch IC to a PCB. The rules and requirements are made available from the evaluation board product designs, which are constructed with standard PCB materials.